REMARKS

Claims 13, 21, 28, and 44 have been amended. Claims 15, 23, and 30 have been canceled. Claims 46-55 have been added. Claims 13-14, 16-22, 24-29, and 31-55 are now pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and following remarks.

Claims 13-17, 19, and 44-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,981,398 ("Tsai") in view of U.S. Patent No. 5,534,462 ("Fiordalice") and U.S. Patent No. 4,722,913 ("Miller"). The rejection is respectfully traversed.

The cited references do not teach or suggest the subject matter of independent claims 13 and 44. Specifically, the references fail to disclose or suggest a semiconductor device comprising: "a layer that is transparent to light having a first thickness, wherein said transparent layer includes a material selected from the group consisting of BPSG, PSG and TEOS; and a first anti-reflective coating formed beneath the transparent layer having a second thickness, wherein said first thickness is greater than the second thickness," as recited in claim 13, or "a semiconductor comprising, *inter alia*, "a silicon oxide layer . . . an anti-reflective coating layer having a first thickness . . . a layer which is transparent to the wavelength of light . . . having a second thickness greater than said first thickness, wherein said transparent layer includes a material selected from the group consisting of BPSG, PSG and TEOS," as recited in claim 44. The cited references, alone or in combination, do not teach or suggest a transparent layer which includes a material selected from the group consisting of BPSG, PSG, and TEOS.

Tsai relates to a "method of forming a chlorine containing plasma etched patterned layer." (Abstract). To this end, Tsai discloses a silicon oxide dielectric layer 13 formed over a blanket target layer 12. (Col. 5, lines 21-24; Figure 1). Next, a "blanket hard mask layer 14 is formed over the silicon oxide dielectric layer 13." (Col. 5, lines 23-24). Tsai, however, "the blanket hard mask layer 14 is formed from a material selected from the group consisting of silsesquioxane spin-on-glass (SOG) materials and amorphous carbon materials." (Col. 6, lines 45-49).

Fiordalice relates to forming "conductive plugs in a semiconductor device without the use of common titanium and titanium nitride glue layers which line the plug opening." (Col. 2, lines 66-67; Col. 3, lines 1-2). To this end, Fiordalice discloses "a conductive plug (46) is formed in a semiconductor device (30) by using an aluminum nitride glue layer (42)." (Abstract). In Fiordalice, a "glue layer is deposited on an interlayer dielectric (40) prior to forming a contact opening (44), such that the glue layer does not line the opening sidewalls or bottom." (Abstract).

Miller relates to "doped semiconductor vias to contacts." (Abstract). Miller discloses that "an undoped wide band-gap semiconductor (18) is used for the insulating layer to isolate the silicon substrate from the metal interconnection pattern." (Abstract). This way, conductive vias are provided "through the insulating layer for connection to the source and drain of the transistors of the circuit." (Abstract).

The subject matter of claims 13-17, 19 and 44-45 would not have been obvious over Tsai in view of Fiordalice and Miller because the Office Action fails to establish a *prima facie* case of obviousness. First, not all claim limitations are taught or suggested by the prior art references, whether considered alone or in combination. None of the references disclose or suggest that the "transparent layer includes a material selected

from the group consisting of BPSG, PSG and TEOS," as recited in independent claims 13 and 44.

Second, there is no motivation to combine Tsai and Fiordalice as the Office Actio suggests, since Tsai teaches away from using other materials such as BPSG, PSG, or TEOS for hard mask layer 14. For example, Tsai discloses that the blanket hard mask layer 14, which arguably corresponds to the transparent layer recited in claims 13 and 44, "is formed from a material selected from the group *consisting of silsesquioxane spin-on-glass (SOG) materials and amorphous carbon materials.*" (Col. 6, lines 45-49) (emphasis added). Tsai's disclosed materials are different from Applicants' claimed BPSG, PSG, and TEOS comprising transparent layer.

Although Fiordalice may disclose that BPSG, PSG, and TEOS can be used as dielectric materials, Tsai teaches away from employing them. In Tsai's col. 6, line 45 through col. 7, line 65, a lengthy discussion is presented regarding the benefits of using only silsesquioxane spin-on-glass (SOG) materials and amorphous carbon materials in Tsai.

Specifically, Tsai teaches that "[a]s is understood by a person skilled in the art, a patterned hard mask layer formed from the blanket hard mask layer 14 of the present invention when formed employing *either* a silsesquioxane spin-on-glass (SOG) material or an amorphous carbon material *provides advantages* in comparison with a patterned hard mask layer formed employing a silicon oxide material as is otherwise *conventionally* employed for forming hard mask layers within microelectronics fabrication." (Col. 7, lines 28-35). The specific advantages are discussed in col. 7, lines 35-65. Miller is relied upon for disclosing that a silicon oxide layer is provided over a surface of a substrate, and adds nothing to rectify the deficiencies associated with Tsai and Fiordalice.

Finally, there is no motivation to combine Tsai with Fiordalice *and* Miller to obtain the subject matter recited in claims 13 and 44. All of the references are directed to solving different problems, and the only commonality shared between all three is the semiconductor substrate on which their respective structures are formed. For instance, the crux of Tsai is forming a chlorine containing plasma etched patterned layer (Abstract). The crux in Fiordalice is forming a conductive plug in a semiconductor devices without the use of titanium and titanium nitride glue layers. (Col. 1, lines 20-22). The crux in Miller is selective implantation with boron of a carbon layer. (Col. 1, lines 63-67). For at least these reasons, a person of ordinary skill in the art would not have been motivated to combine Tsai with Fiordalice and Miller since the subject matter disclosed in each reference differs greatly from each other.

Claims 14, 16-17, and 19 depend from claim 13 and should be similarly allowable for at least the reasons provided above with regard to claim 13, and on their own merits. Claim 45 depends from claim 44 and should be similarly allowable for at least the reasons provided above with regard to claim 44, and on its own merits.

Claims 21-24, 26, 28-31, 36, and 44-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Fiordalice and Miller, and further in view of Applicants' Own Admission in the Present Specification. The rejection is respectfully traversed.

For similar reasons provided above, Tsai, Fiordalice, and Miller do not teach or suggest that the "transparent layer includes a material selected from the group consisting of BPSG, PSG and TEOS," as recited in independent claims 21, 28 and 44, much less "a layer that is transparent to light having a wavelength of approximately 365 nm," as recited in claim 21, or "a layer that is transparent to light having a wavelength of approximately 193 nm," as recited in claim 28. As discussed previously,

the cited references, alone or in combination, simply do not teach or suggest a transparent layer that comprises BPSG, PSG, or TEOS.

Further, there is no motivation to combine Tsai, Fiordalice, and Miller since the references teach away from each other. Tsai discloses employing either a silsesquioxane spin-on-glass (SOG) material or an amorphous carbon material which provides advantages over other dielectric materials. Thus, the teachings of Fiordalice would not have been combined with Tsai. Still further, the references are directed to entirely different inventions and the only commonality shared is their respective semiconductor substrates. Applicants' own admission is relied upon for disclosing DUV (248 nm), mid-UV (365 nm), and extreme UV (193 nm), and adds nothing to rectify the deficiencies of Tsai, Fiordalice, and Miller.

The Office Action asserts that it would have been obvious to expose the photoresist of Tsai to light at a wavelength of 193 nm or 365 nm. Applicants respectfully disagree. Tsai discloses that "the series of patterned photoresist layers 16a, 16b, and 16c is preferably formed employing a deep ultraviolet (DUV) photoexposable photoresist material to form the series patterned photoresist layers 16a, 16b, and 16c having a minimum linewidth W1 and/or a minimum aperture width W2 of from about .25 to about 1.0 microns." (Col. 8, lines 9-18).

Accordingly, the "thickness of the patterned photoresist layers 16a, 16b, and 16c is typically limited to no greater than about 8000 angstroms, due to depth of focus limitations of an advanced photoexposure apparatus employed when photoexposing a corresponding blanket photoresist layer employed when forming the series of patterned photoresist layers 16a, 16b, and 16c." (Col. 8, lines 18-24).

In other words, a specific advanced photoexposure apparatus, *i.e.*, a DUV emitting apparatus, is used in Tsai to develop the patterned photoresist layers 16a, 16b, and 16c. This in turn, allows the photoresist layers 16a, 16b, and 16c to have the required minimum linewidth W1 and aperture width W2 of from about .25 to about 1.0 microns. There is no motivation to employ another light emitting apparatus in Tsai, *i.e.*, a mid-UV or extreme UV apparatus, since this would change the linewidths W1 and aperture width W2 of photoresist layers 16a, 16b, and 16c.

Claims 22, 24, and 26 depend from claim 21 and should be similarly allowable for at least the reasons provided above with regard to claim 21, and on their own merits. Claims 29 and 31 depend from claim 28 and should be similarly allowable for at least the reasons provided above with regard to claim 28, and on their own merits. Claim 45 depends from claim 44 and should be similarly allowable for at least the reasons provided above with regard to claim 44, and on its own merits.

Claims 18, 20, 25, 27, 32, 34-35, and 37-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsai in view of Fiordalice, Miller and Applicants' Own Admission, and further in view of U.S. Patent No. 5,741,626 ("Jain"). The rejection is respectfully traversed.

For similar reasons provided above, Tsai, Fiordalice, Miller, and Applicants' Own Admission, do not teach or suggest that the "transparent layer includes a material selected from the group consisting of BPSG, PSG and TEOS," as recited in independent claims 13, 21, 28 and 44, much less "a layer that is transparent to light having a wavelength of approximately 365 nm," as recited in claim 21, or "a layer that is transparent to light having a wavelength of approximately 193 nm," as recited in claim 28. As discussed previously, the cited references, alone or in combination, simply do not teach or suggest a transparent layer that comprises BPSG, PSG, or TEOS. The cited

references do not teach or suggest a layer that is transparent to light having a wavelength of approximately 365 nm or 193 nm.

Further, there is no motivation to combine Tsai, Fiordalice, Miller, and Applicants' Own Admission since the references teach away from each other. Tsai discloses employing either a silsesquioxane spin-on-glass (SOG) material or an amorphous carbon material which provides advantages over other dielectric materials. There is no motivation to combine it with Fiordalice. Tsai also discloses a DUV apparatus and there is no motivation to employ a different light wavelength since this would change the resulting width and apertures of photoresists 16a, 16b, and 16c. Still further, Tsai, Fiordalice, and Miller are directed to entirely different inventions and the only commonality shared is their respective semiconductor substrates.

Jain is relied upon for disclosing the use of silicon nitride as an ARC and also the use of a second antireflective layer; but, adds nothing to rectify the deficiencies associated with Tsai, Fiordalice, Miller, and Applicants' Own Admission. For example, there is no motivation to combine Tsai with Jain.

Jain discloses a method of forming a *dual damascene* structure by using "a dielectric phase tantalum nitride (Ta_3N_5) anti-reflective coating (ARC) layer." (Col. 2, lines 50-53). Tsai, in contrast, discloses a "method of forming a chlorine containing plasma etched patterned layer." (Abstract). Tsai's hard mask layer 14 is formed of either silsesquioxane spin-on-glass (SOG) materials or amorphous carbon materials. It is <u>not</u> formed of tantalum nitride. Accordingly, there is no motivation to combine these references since Tsai teaches away from the proposed combination. The proposed combination would require Tsai to undergo a major redesign and reconstruction to incorporate the tantalum nitride ARC layer, since Tsai's hard mask layer 14 would no

longer be formed of silsesquioxane spin-on-glass (SOG) materials or an amorphous carbon material.

Claims 18, 20, 35, and 37 depend from claim 13 and should be similarly allowable for at least the reasons provided above with regard to claim 13, and on their own merits. Claims 25, 27, and 38-40 depend from claim 21 and should be similarly allowable for at least the reasons provided above with regard to claim 21, and on their own merits. Claims 32 , 34, and 41-43 depend from claim 28 and should be similarly allowable for at least the reasons provided above with regard to claim 28, and on their own merits. Claim 45 depends from claim 44 and should be similarly allowable for at least the reasons provided above with regard to claim 44, and on its own merits.

Applicants respectfully submit that the subject matter of newly added claims 46-55 is not disclosed or suggested by the prior art of record. The prior art of record does not disclose or suggest a semiconductor device comprising, *inter alia*, "a gate electrode . . . a first impurity region . . . a second impurity region . . . an interconnection layer . . . a first dielectric anti-reflective coating layer . . . and an interlayer insulation film . . . wherein a contact hole is provided through said first anti-reflective coating layer and said interlayer insulation film exposing said second impurity region," as recited in claim 46.

Similarly, the prior art of record does not disclose or suggest a method of forming a semiconductor device, *inter alia*, by "forming a gate electrode . . . forming a first impurity region . . . forming a second impurity region . . . forming an interconnection layer . . . forming a first anti-reflective coating layer . . . forming layer which is transparent to light . . . forming a photosensitive film layer . . . forming a mask layer . . . and exposing said photosensitive film layer and said mask layer to a

wavelength of light, wherein said step of exposing forms a contact hole through said layers to expose said second impurity region," as recited in claim 52.

Applicants' claimed invention relates to a method that produces a structure with reduced amount of notching during a photolithographic process. The topography of the underlying structures beneath the first anti-reflective coating layer is typically non-planar. The complex refractive index of the first anti-reflective layer is selected to minimize the amount of reflected light from the non-uniform structures. The cited references do not teach or suggest the claimed subject matter recited in claims 46 and 52.

For example, Tsai merely discloses a method of forming a chlorine containing plasma etched layer (FIG. 1). Tsai does not disclose underlying non-uniform structures such as a gate electrode with a first and second impurity region, much less forming a contact hole through multiple layers. The reflected light from non-uniform structures in or on semiconductor substrate 10, is not a concern since a target blanket layer (12) 5000 to 9000 Å thick is formed entirely over the surface. Only then, is the *optional* blanket silicon oxide layer (13) formed on the target blanket layer (12). Then, a *hard mask* layer is formed on the silicon oxide layer (13). The photoresist layer 16a, 16b, and 16c is exposed to form the structure in FIG. 2. However, the target blanket layer (12) is *not* etched through to the semiconductor substrate. For at least these reasons, the cited references do not disclose or suggest a method or structure with a contact hole that is provided through said first anti-reflective coating layer and said interlayer insulation film exposing said second impurity region.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorney for Applicants